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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/085,919 | 02/28/2002 | Albrecht Mayer | J&R-0819 | 1176 |

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| EXAMINER | |
|---|---|
| BRITT, CYNTHIA H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/085,919 | MAYER ET AL. | |
| | Examiner | Art Unit | |
| | Cynthia Britt | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12 and 13* is/are allowed.

6)☒ Claim(s) *1-4 and 10--11* is/are rejected.

7)☒ Claim(s) *5-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## *DETAILED ACTION*

Claims 1-8 and 10-13 are presented for examination.

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 12, 2005 has been entered.

### *Drawings*

In order to avoid abandonment, the drawing informalities (newly submitted drawing requires figure number) noted in the paper mailed on May 4, 2005, must now be corrected. Correction can only be effected in the manner set forth in the above noted paper.

### *Claim Objections*

The following is a quotation of 37 CFR § 1.75(i):

(i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

Claims 1, 8, and 12-13 are objected to for containing a plurality of elements or steps that are not separated by a line indent. An amendment is required to put the

claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements.

### *Allowable Subject Matter*

Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Specification*

The disclosure is objected to because of the following informalities: the newly added figure must be appropriately referenced within the specification and must be included in "Brief Description of the Drawings" on page 9.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 8 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 8 states in part "In an error determination method where..." this statement defines the environment in which the

claimed invention is intended to occur or operate, but fails to recite a method or system that falls into a statutory category of invention.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8, and 10-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 is unclear as to the intended metes and bounds of what is sought to be patented (Note 35 U.S.C. 101 rejection above).

Claims 10 and 11 are dependent upon claim 8 and therefore inherit the 35 U.S.C. 112, second paragraph issues of the independent claim.

***Response to Arguments***

Applicant's arguments filed April 12, 2005 have been fully considered but they are not persuasive.

In response to applicant's argument that "the "scan paths" of Spix et al. have virtually nothing in common with the "scan chains" of the instantly claimed method", a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably

distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and In re Otto, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

Applicant also states, "claim 8 is an In re Dean claim, which is in effect a combination/subcombination claim. The differences between a simple combination claim and a combination/subcombination claim were highlighted in the last response and reference is made thereto." The examiner has been unable to locate any reference to an In re Dean claim either on the USPTO site the MPEP or on the internet. Therefore, if Applicant continues to put forth this argument, the examiner requests either a copy of or a citation for In re Dean. The examiner also fails to recognize any "differences between a simple combination claim and a combination/subcombination claim" which applicant suggests were highlighted in the previous response. The examiner also requests a further explanation of such and/or at least point out where in the previous response this explanation was highlighted.

As per applicant's argument, "...a program-controlled unit that uses scan chains with a plurality of elements. These same elements are the elements used in the program control unit itself. In other words, the program control unit processes a program, i.e. it is operated under program control, and when a certain pre-determined error is detected, the elements of the program control units are frozen and connected to scan chains and the scan chains then are read out." The examiner would like to point

out that Spix et al. column 8 lines 17-56 is merely describing the standard feature (capture shift update) of a typical scan path. Once data is shifted out of a scan register, new data is shifted into the place of what is shifted out. The prior art is replete with references that describe this in more detail than Spix et al. (such as the currently cited references) but this is however how scan paths typically work.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 8 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Spix et al. U.S. Patent No. 5,253,359.

As per claim 1, Spix et al. teach a control and maintenance architecture providing an integrated hardware and software solution to the problem (program controlled unit) of access to and control over the internal machine registers of a highly parallel multiprocessor system (Column 3 lines 34-38). The use of scan path elements and functions are implemented (Column 8 lines 17-20). If an error (predetermined event) is detected in the clusters, machine state information is saved by the scan paths, and is gathered by the MCUs. It is important that the information is read from the scan paths by the MCUs as quickly as possible, since a subsequent error in the cluster may

overwrite the previous error before it can be gathered. For example, if a single bit memory error is detected, the scan paths can latch (unable to change states) the entire machine state for (output scan chain contents) subsequent analysis (Column 8 lines39-48).

As per claims 2 and 3, Spix et al. teach controlling the operation of the system such as starting, stopping (deactivating), or n-stepping the master clock (supplying clock signals), setting or sensing internal machine states, executing diagnostic routines, and capturing errors (predetermined event) at run-time (on chip debug support) for later display and analysis (Column 2 lines 26-36).

As per claim 4, Spix et al. teach that an operator can control (from outside) the operation of the system such as starting, stopping, or n-stepping the master clock, setting or sensing internal machine states, executing diagnostic routines, and capturing errors at run-time for later display and analysis (Column 2 lines 26-36).

As per claims 8 (as best understood by the examiner) and 10, Spix et al. teach a control and maintenance architecture providing an integrated hardware and software solution (program controlled unit) to the problem of access to and control over the internal machine registers of a highly parallel multiprocessor system. (Column 3 lines 34-38) The use of scan path elements and functions are implemented (Column 8 lines 17-20). If an error (predetermined event) is detected in the clusters, machine state information is saved by the scan paths, and is gathered by the MCUs. It is important that the information is read from the scan paths by the MCUs as quickly as possible, since a subsequent error in the cluster may overwrite the previous error before it can be

gathered. For example, if a single bit memory error is detected, the scan paths can latch (unable to change states) the entire machine state for subsequent analysis (Column 8 lines39-48)

As per claim 11, Spix et al. also teach that an operator can control the operation of the system such as starting, stopping, or n-stepping the master clock, setting or sensing internal machine states, executing diagnostic routines (comparing data), and capturing errors at run-time (from reading the outputs of the scan chains) for later display and analysis (Column 2 lines 26-36).

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 20030097614 A1 Rajski et al.

This application teaches in the background of invention section, that the sequential logic is used as scan cells that can be configured into scan chains during testing of the circuit. A typical scan cell contains a two-input multiplexer followed by a sequential or memory element such as a flip-flop. The flip-flop is an edge-triggered sequential element where input data is latched into the element at the active edge of the clock signal. The multiplexer control signal (known as scan enable, or SE) determines the mode of operation for the scan cells during test: scan or capture. In scan mode, the scan cells are connected in series to form a scan chain and the combinational logic is

decoupled from the scan chain. Test stimulus in the form of a test vector of data is brought in from a source such as a PRPG and clocked into the scan chain. In capture mode, data is propagated from input scan cells through functional paths of the combinational logic and captured in output scan cells (which may be the same as or different from the input scan cells). Capture mode exercises the logic's functional paths and hence performs testing of the faults in these structures. After capture, the scan enable changes the cell operation back to scan mode and the captured data is shifted out. Page 1 paragraph [0008].

U.S. Patent No. 5,453,992 Whetsel

This patent teaches that the instruction scan mode is achieved by sequencing the TAP through a series of states. During the instruction scan mode, the instruction register receives control from the TAP to perform a predefined set of test steps, comprising; (1) a capture step, (2) shift step, and (3) an update step. The capture step causes the instruction register to parallel load with status information. The shift step causes the instruction register to shift data from TDI to TDO. The update step causes the instruction register to parallel output the instruction data it received during the shift step. (Figure 2, column 2 lines 43-54)

U.S. Patent No. 4,503,537 McAnney

This patent further teaches that the LSSD scan paths of each logic circuit chip on a circuit module are connected to additional test circuit chips on the same module. The

test chips contain a random signal generator and data compression circuit to perform random stimuli signature generators and also contain switching circuits to connect the scan paths of the chips in parallel between different stages of the random signal generator and the data compression means for random stimuli signature generators and to disconnect the scan paths from the signal generator and data compression circuitry and arrange them serially in a single scan path to perform other tests. See claims 1-3, Abstract.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133